## CLAIMS

1. A method for testing a first integrated circuit chip which is packaged along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are shared by the first and second integrated circuit chips, the method comprising:

powering down the second integrated circuit chip;

tri-stating a plurality of input/output (I/O) drivers of the second integrated circuit chip so that the plurality of I/O drivers do not drive any signals onto any connections for the shared external terminals; and

performing testing of the first integrated circuit chip according to one or more regular testing routines.

2. The method of claim 1 wherein powering down the second integrated circuit chip comprises:

placing the second integrated circuit chip into a test mode;

setting a predetermined test code; and

loading the predetermined test code into at least one register of the second integrated circuit chip.

3. The method of claim 1 wherein powering down the second integrated circuit chip comprises transitioning the first integrated circuit chip from normal operation into test mode.

4. The method of claim 1 wherein performing testing of the first integrated circuit chip comprises measuring a standby current of the first integrated chip.

5. The method of claim 1 comprising pre-charging the first integrated circuit chip.

6. The method of claim 1 wherein the first integrated circuit chip comprises a logic device and wherein the second integrated circuit chip comprises a memory device.

7. A system for testing a first integrated circuit chip packaged along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are shared by the first and second integrated circuit chips, the system comprising:

means for powering down the second integrated circuit chip;

means for tri-stating a plurality of input/output (I/O) drivers of the second integrated circuit chip so that the plurality of I/O drivers do not drive any signals onto any connections for the shared external terminals; and

means for performing testing of the first integrated circuit chip according to one or more regular testing routines.

8. The system of claim 7 wherein means for powering down the second integrated circuit chip comprises means for transitioning the first integrated circuit chip from normal operation into test mode.

9. The system of claim 7 wherein means for performing testing of the first integrating circuit chip comprises means for measuring a standby current of the first integrated chip.

10. The system of claim 7 wherein the first integrated circuit chip comprises a logic device and wherein the second integrated circuit chip comprises a memory device.

11. A method for setting up a first integrated circuit chip to allow for testing of a co-packaged second integrated circuit chip, wherein the first integrated circuit chip is designed for normal operation and a test mode, the method comprising:

transitioning the first integrated circuit chip from normal operation into test mode;

entering a test code into the first integrated circuit chip for disabling at least one circuit in the first integrated circuit chip so that only minimal current flows through the first integrated circuit chip; and

pre-charging the first integrated circuit chip.

12. The method of claim 11 wherein entering a test code comprises:

receiving a test code at an external terminal for a semiconductor device in which the first integrated circuit chip and the second integrated circuit chip are packaged;

setting a test code; and

loading the test code into the first integrated circuit chip.

13. The method of claim 11 wherein the first integrated circuit chip comprises a memory device and wherein the second integrated circuit chip comprises a logic device.

14. The method of claim 13 wherein pre-charging the first integrated circuit chip comprises closing a page of the memory device.

15. A system comprising:

a first integrated circuit chip packaged in a semiconductor device;

a second integrated circuit chip packaged along with the first integrated circuit chip in the same semiconductor device;

at least one external terminal for the semiconductor device shared by the first and second integrated circuit chips for the transfer of signals between the first or second integrated circuit chip and circuitry external to the semiconductor device;

wherein in a first mode of operation for the semiconductor device signals are transferred between the first and second integrated circuit chips, and wherein in a second mode of operation for the semiconductor device signals are not transferred between the first and second integrated circuit chips and a standby current of the first integrated circuit chip is measured via the at least one shared external terminal; and means for putting the second integrated circuit chip into a condition so that the second integrated circuit chip does not interfere with measurement of the standby current of the first integrated circuit chip.

16. The system of claim 15 wherein the means for putting the second integrated circuit chip into a condition comprises means for powering down the second integrated circuit chip.

17. The system of claim 15 wherein the means for putting the second integrated circuit chip into a condition comprises means for tri-stating one or more input/output (I/O) drivers of the second integrated circuit chip.

18. The system of Claim 15 wherein the second integrated circuit chip comprises a memory device.

19. The system of Claim 15 wherein the second integrated circuit chip comprises a logic device.